



# Asian Test Symposium 2026

December 1-3, 2026 | Kaohsiung, Taiwan



## Call for Papers

The 35<sup>th</sup> Asian Test Symposium (ATS 2026), a premier international forum in the field of electronics testing, will be held at the Hotel Nikko Kaohsiung in Taiwan. This conference serves as a pivotal platform for academic researchers and industry professionals from around the globe. Its primary objective is to facilitate the exchange of groundbreaking ideas and the presentation of the latest research findings. We cordially invite the submission of original papers covering all aspects of system, module, and device testing, as well as broader test technologies.

### **General Chair:**

Jing-Jia Liou  
(National Tsing Hua University, Taiwan)

### **Program Chair:**

Tong-Yu Hsieh  
(National Sun Yat-sen University, Taiwan)

### **Finance Chair:**

Jiun-Lang Huang  
(National Taiwan University, Taiwan)

### **Local Arrangement Chair:**

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### **Registration Chair:**

Hao-Chiao Hong  
(National Yang Ming Chiao Tung University, Taiwan)

### **Publicity Chair:**

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(National Central University, Taiwan)

### **Publication Chair:**

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(National Chung Hsing University, Taiwan)

### **Tutorial Chair:**

Charles H.-P. Wen  
(National Yang Ming Chiao Tung University, Taiwan)

### **North American Liaison:**

Krishnendu Chakrabarty  
(Arizona State University, United States of America)

### **European Liaison:**

Ilija Polian  
(University of Stuttgart, Germany)

## Scope

Topics of interest include (but are not limited to):

- AI test and Test for AI
- Analog/Mixed-Signal Test
- ATE Design
- Automatic Test Pattern Generation (ATPG)
- Autonomous Testing
- Board-Level Testing and Diagnosis
- Boundary Scan Test
- Built-In Self-Test (BIST)
- CPU/GPU Test
- Connectivity Testing
- Defect-Based Test
- Delay and Performance Test
- Dependability and Functional Safety
- Design Verification, Validation, and Debug
- Design for Testability (DFT)
- Diagnosis and Silicon Debug
- Fault Diagnosis and Failure Analysis
- Fault Modeling and Simulation
- Fault Tolerance
- Hardware Oriented Security and Trust
- High-Speed I/O Test
- Heterogeneous Testing
- Low-Power IC Test
- Machine Learning in Test
- Memory Test, Diagnosis, and Repair
- Multi-/Many-core Processor Test
- Online Test
- On-Chip Measurement
- Power/Thermal/Reliability Issues in Test
- Reconfigurable System Test
- Reliability and Testing for Emerging/Approximate/Quantum Computing
- RF Test
- Safety and Test for Automotive ICs
- Self-Repair
- SiP, Chiplet, 2.5D and 3D IC Test
- Software Test and Reliability
- Standards in Test
- System-on-Chip Test
- Test Compression
- Test Economics
- Test Quality
- Test Synthesis
- Test for Biomedical Circuits and Systems
- Test for MEMS and Microfluidic Systems
- Test for Nanoscale Devices and Emerging Technologies
- Test for Reversible and Quantum Circuits
- Test for Sensors and IoT
- Yield Analysis, Learning, and Enhancement

## Paper Submission

The ATS 2026 Organizing Committee invites original, unpublished paper submissions on the above topics. Regular paper submissions should be made electronically by PDF manuscripts only, not exceeding 6 pages in IEEE 2-column format (including abstract, figures, tables, and bibliography). A submission will be considered evidence that upon acceptance, at least one author will attend the conference to make the presentation. Authors of accepted papers are also responsible for preparing the final manuscripts in time to be included in the electronic proceedings, which will eventually be published in IEEE Xplore Digital Library. At least one full registration to the conference is required for each accepted paper. More information is available from the following link: <https://www.ats2026.tw>

## Key Dates

- Submission deadline: **June 6, 2026**
- Notification of acceptance: **Sept. 14, 2026**
- Camera ready manuscript: **Oct. 13, 2026**



[www.ats2026.tw](https://www.ats2026.tw)

